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# INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Complete if Known

Application Number **09/976,983**  
 Filing Date **10/12/2001**  
 First Named Inventor **Xiaoqin Deng, et al.**  
 Group Art Unit **2518**  
 Examiner Name **PHAN**  
 Attorney Docket No. **T-31071**

Sheet **1** of **1**

## U.S. PATENT DOCUMENTS

| Exam. Initials* | Cite No.  | U.S. Patent Document |                                   | Name of Patentee or Applicant of Cited Doc. | Date of Pub. of Cited Doc. (mm-dd-yyyy) | Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear |
|-----------------|-----------|----------------------|-----------------------------------|---|---|---|
|                 |           | Number               | Kind Code <sup>2</sup> (if known) |   |   |   |
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|                 | <b>AB</b> |                      |                                   |   |   |   |
|                 | <b>AC</b> |                      |                                   |   |   |   |
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## FOREIGN PATENT DOCUMENTS

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|                 | <b>BB</b> |                         |                     |                                   |   |   |   |                |
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|                 | <b>BG</b> |                         |                     |                                   |   |   |   |                |
|                 | <b>BH</b> |                         |                     |                                   |   |   |   |                |
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## OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

| Exam. Initials* | Cite No.  | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published. | T <sup>3</sup> |
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| <b>TP</b>       | <b>CA</b> | <b>NODA, K., et al., "A 1.8-μm<sup>2</sup> Loadless CMOS Four-Transistor SRAM Cell in a 0.18-μm Logic Technology," 1998 IEEE, pp. 643-646</b>   |                |
| <b>TP</b>       | <b>CB</b> | <b>NODA, K., "An Ultra-High-Density High-Speed Loadless Four-Transistor SRAM Macro with a Dual-Layered Twisted Bit-Line and a Triple-Well Shield," 2000 IEEE Custom Integrated Circuits Conference, pp. 283-286</b>   |                |
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